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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/623,101	07/18/2003	Guillermo Rozas	TRAN-P072	2896

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WAGNER, MURABITO & HAO LLP
Third Floor
Two North Market Street
San Jose, CA 95113

EXAMINER	
RIZZUTO, KEVIN P	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 12/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/623,101	ROZAS ET AL.	
	Examiner	Art Unit	
	Kevin P. Rizzuto	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *7/18/03 and 5/17/04*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 July 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-14 have been examined.

2. Acknowledgement of papers filed: application on 7/18/05 and oath/declaration on 5/17/05. The papers filed have been placed on record.

Drawings

3. The drawings are objected to for the reasons specified in the attached Draftsperson's Review. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

4. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-3, 5-7 and 10-12 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Larson, U.S. Patent 5,115,500.

7. As per claim 1, Larson teaches a method of processing an instruction, said method comprising:

a. Fetching said instruction using a corresponding address from a memory unit: [An instruction is fetched from the I-Store 2 using an address from the memory unit (Instruction Address Register, IAR 3). (Fig. 2, col. 5, line 34 to col. 6, line 40)]

b. Wherein a plurality of possible meanings are associated with said instruction: [There are a possibility of a plurality of meanings for each

instruction depending on the concatenated address bits. (Fig. 2, col. 5, line 34 to col. 6, line 40)]

c. Concatenating a portion of said corresponding address to said instruction to form an extended instruction: [IDSR and IDR is a concatenation of a portion of the address bits and the instruction fetched, which forms an extended instruction. (Fig. 2, col. 5, line 34 to col. 6, line 40)]

d. And executing said extended instruction, wherein said portion of said corresponding address determines a meaning for said extended instruction from said possible meanings: [The instruction is decoded and then executed with one of the possible meanings, which is dependent on the extended instruction formed from the concatenation. (Fig. 2, col. 5, line 34 to col. 6, line 40)]

8. As per claim 2, Larson teaches the method as recited in Claim 1 wherein said portion is an address bit. (Fig. 2, col. 5, line 34 to col. 6, line 40)]

9. As per claim 3, Larson teaches the method as recited in Claim 1 wherein said portion is a plurality of address bits. (Fig. 2, col. 5, line 34 to col. 6, line 40)]

10. As per claim 5, Larson teaches a method of handling an instruction, said method comprising:

e. Generating said instruction, wherein a plurality of possible meanings are associated with said instruction: [Instructions reside in the I-Store 2 (fig. 2), there are present, therefore they were inherently generated. Each instruction has a plurality of meanings associated with it,

dependent on the corresponding address at which it is stored. (Col. 3, lines 15-22, and col. 5, line 34 to col. 6, line 40.)]

f. Storing said instruction at a particular address in a memory unit such that a portion of said particular address enables determination of a meaning for said instruction from said possible meanings: [Fig. 2, col. 2, lines 21-54 and col. 5, line 34 to col. 6, line 40.]

g. And before executing said instruction, fetching said instruction using said particular address from am memory unit and concatenating said portion of said particular address to said instruction: [Fig. 2, col. 3, lines 52-64 and col. 5, line 34 to col. 6, line 40.]

11. As per claim 6, given the similarities between claim 6 and claim 2, the arguments as stated for the rejection of claim 6 also apply to claim 2.

12. As per claim 7, given the similarities between claim 7 and claim 3, the arguments as stated for the rejection of claim 7 also apply to claim 3.

13. As per claim 10, given the similarities between claim 10 and claim 1, the arguments as stated for the rejection of claim 10 also apply to claim 1.

14. As per claim 11, given the similarities between claim 11 and claim 2, the arguments as stated for the rejection of claim 2 also apply to claim 11.

15. As per claim 12, given the similarities between claim 12 and claim 3, the arguments as stated for the rejection of claim 3 also apply to claim 12.

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. Claims 4, 8-9 and 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Larson, U.S. Patent 5,115,500.

18. As per claim 4, Larson teaches the method as recited in Claim 1 wherein said plurality of possible meanings are specified by the extended instruction. However, Larson fails to teach specific examples of instructions, the invention is taught with generic examples, such as "type 1" and "type 2" instructions, but does not state what functions the instructions specifically perform. Therefore, Larson fails to teach wherein the plurality of possible meanings include an integer type of instruction and a floating point type of instruction.

19. However, Examiner takes Official Notice that integer type and floating point type instructions are well known in the art and required by many programs and are present in the vast majority of instructions, and therefore are included in machine languages and capable of being executed by processors.

20. It would have been obvious to one of ordinary skill in the art at the time the invention was made to decode some instructions as integer and floating point instructions, and in the system of Larson, this would inherently mean the address is used to give the integer or floating point instruction this meaning out of a

plurality of possible meanings, since Examiner takes Official Notice integer and floating point instructions are well known instructions in instruction sets.

21. As per claim 8, given the similarities between claim 8 and claim 4, the arguments as stated for the rejection of claim 4 also apply to claim 8.

22. As per claim 13, given the similarities between claim 13 and claim 4, the arguments as stated for the rejection of claim 4 also apply to claim 13.

23. As per claim 9, Larson is silent on specifically how the instructions are generated and stored in the memory in the specific locations. While Larson describes that high-level programs are compiled before inherently being placed in an instruction memory for execution (Col. 1, lines 11-29), and that the instructions are stored in specific locations so as to define the decoding of the instructions, Larson does not specifically state that the I-Store 2 contains instructions compiled from high-level code, which were generated and stored by use of the compiler. Therefore, while Larson teaches all the actions taken by the compiler, that is, the instructions are generated and stored at specific locations, Larson fails to teach a compiler performs these actions.

24. However, Examiner takes Official Notice that compilers are used to generate and store instructions in memory, so as to allow programmers to write code in high level languages and allow the compiler to convert and prepare the code for execution by a processor.

25. It would have been obvious to one of ordinary skill in the art at the time the invention was made to perform the generating and storing of the instructions using a compiler since Examiner takes Official Notice compilers are well known

in the art and allow programmers to write code in high-level languages instead of machine code.

26. As per claim 14, given the similarities between claim 14 and claim 9, the arguments as stated for the rejection of claim 9 also apply to claim 14.

Conclusion

27. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin P Rizzuto whose telephone number is (571) 272-4174. The examiner can normally be reached on M-F, 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KPR

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100